IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Currently Amended) A multi-stage mixer module, comprising:

a transconductance block for receiving an input signal having a frequency, the transconductance block for converting the input signal from a voltage to a current to produce a first mixing stage input signal in a current domain;

a first frequency mixing stage coupled to receive a first reference signal and the first mixing stage input signal, the first mixing stage producing a second mixing stage input signal in the current domain ~~wherein the input signal comprises a frequency correction input for mixing with the uncompensated local oscillation signal frequency to produce a frequency compensated local oscillation signal~~;

a second frequency mixing stage coupled to receive a second reference signal and the second mixing stage input signal, the second mixing stage producing a second mixing stage output signal in the current domain wherein a sum of a frequency value of the first reference signal, when added to a frequency value of the second reference signal, is equal to an uncompensated local oscillation signal frequency value; and

an output stage coupled to receive the second mixing stage output signal, the output stage for converting the second mixing stage output signal from the current domain to a voltage domain to produce a mixer module output signal.

2. (Original) The multi-stage mixer module of claim 1 wherein the first reference signal is characterized by a frequency that is twice a frequency of the second reference signal.

3. (Original) The multi-stage mixer module of claim 1 wherein the second reference signal is characterized by a frequency that is twice a frequency of the first reference signal.

4. (Canceled)

5. (Currently amended) The multi-stage mixer module of claim 1 wherein the input signal comprises a frequency correction input for mixing with the uncompensated local oscillation signal frequency to produce a frequency compensated local oscillation signal.

6. (Original) A radio frequency (RF) transceiver integrated circuit, comprising:

a local oscillator that generates an RF local oscillation signal corresponding to an RF channel;

a receiver section operably coupled to the local oscillator to receive the RF local oscillation signal, wherein the receiver section receives an incoming RF signal, and wherein the receiver section down-converts the incoming RF signal based upon the RF local oscillation signal to produce an incoming baseband signal;

a transmitter section operably coupled to the local oscillator to receive the RF local oscillation signal, wherein the transmitter section receives an outgoing baseband signal, and wherein the transmitter section up-converts the outgoing baseband signal to produce an outgoing RF signal; and

wherein the local oscillator further comprises:

a phase locked loop that generates a phase locked loop oscillation signal;

a divider circuit that receives the phase locked loop oscillation signal to produce a divided phase locked loop oscillation signal; and

a two step mixing stage that receives phase the locked loop oscillation signal, the divided phase locked loop oscillation signal and a frequency correction input, wherein the two step mixing stage:

converts the frequency correction input to a current to create a frequency correction input in the current domain;

mixes the frequency correction input in the current domain with the divided phase locked loop oscillation signal to create a local oscillation frequency correction component; and

mixes the local oscillation frequency correction component with the phase locked loop oscillation signal to produce a frequency corrected local oscillation signal.

7. (Original) The RF transceiver integrated circuit of claim 6 wherein the divider circuit produces a divided phase locked loop oscillation signal having a frequency that is one half of the phase locked loop oscillation signal.

8. (Original) The RF transceiver integrated circuit of claim 6 wherein the divider circuit produces a divided phase locked loop oscillation signal having a frequency that is one third of the phase locked loop oscillation signal.

9. (Original) The RF transceiver integrated circuit of claim 6 wherein a sum frequency value of a frequency value of the divided phase locked loop oscillation signal and a frequency value of the phase locked loop oscillation signal is equal to a desired uncompensated local oscillation frequency value.

10. (Currently Amended) The RF transceiver integrated circuit of claim [[1]]6, wherein the frequency correction input is received from a coupled baseband processor.

11. (Currently Amended) The RF transceiver integrated circuit of claim [[1]]6, further comprising a baseband processor, wherein:

the baseband processor is coupled to receive an incoming baseband signal;

the baseband processor determines the frequency correction input from the incoming baseband signal; and

the baseband processor provides the frequency correction input to the local oscillator.

12. (Original) In a Radio Frequency (RF) transceiver mixer module, a method for down-converting a received RF signal, comprising:

producing a baseband signal to a baseband processor;

recciving a frequency correction input from the baseband processor;

receiving an uncompensated divided local oscillation signal;

mixing the uncompensated divided local oscillation signal with the frequency correction input in a first mixing stage to produce a local oscillation frequency correction current signal component;

receiving an undivided and uncompensated local oscillation signal;

mixing the undivided and uncompensated local oscillation signal with the local oscillation frequency correction current component in a second mixing stage to produce a frequency corrected local oscillation current signal;

converting the frequency corrected local oscillation signal to a voltage signal; and

mixing the frequency corrected local oscillation voltage signal either with the received RF signal to produce the baseband signal or with a baseband signal to produce an RF signal.

13. (Original) The method of claim 12 further including the step of dividing the undivided and uncompensated local oscillation signal to produce the uncompensated divided local oscillation signal.

14. (Original) The method of claim 12 wherein the local oscillation frequency correction component is produced to the second mixing stage without converting the local oscillation frequency correction component from the current domain to the voltage domain.

15. (Original) The method of claim 12 wherein the two mixing steps occur without converting signals between the current and voltage domains.

16. (Original) A radio frequency (RF) transceiver integrated circuit, comprising:

a local oscillator that generates an RF local oscillation signal corresponding to an RF channel;

a receiver section operably coupled to the local oscillator to receive the RF local oscillation signal, wherein the receiver section receives an incoming RF signal, and wherein the receiver section down-converts the incoming RF signal based upon the RF local oscillation signal to produce an incoming baseband signal;

a transmitter section operably coupled to the local oscillator to receive the RF local oscillation signal, wherein the transmitter section receives an outgoing baseband signal, and wherein the transmitter section up-converts the outgoing baseband signal to produce an outgoing RF signal; and

wherein the local oscillator further comprises:

a phase locked loop that generates a phase locked loop oscillation signal;

a divider circuit that receives the phase locked loop oscillation signal to produce a divided phase locked loop oscillation signal; and

a two step mixing stage that receives phase the locked loop oscillation signal, the divided phase locked loop oscillation signal and a frequency correction input, wherein the two step mixing stage further includes:

a transconductance block that includes a first MOSFET having a source terminal coupled to a current sink, the first MOSFETS having a gate terminal coupled to receive a frequency correction input wherein the first MOSFET converts the frequency correction input to a current to create a frequency correction input in the current domain;

first and second mixer MOSFETs, the first and second mixer MOSFETs having commonly connected source terminals that are further coupled to a drain terminal of the first MOSFET and further including a drain terminal and a gate terminal wherein the first mixer MOSFET receives a divided phase locked loop oscillation signal and mixes the frequency correction input in the current domain with the divided phase locked loop oscillation signal received at the gate terminal to create a local oscillation frequency correction component at the drain terminal of the first mixer MOSFET; and

third and fourth mixer MOSFETS having commonly connected source terminals that are further coupled to a drain terminal of the first mixer MOSFET and further including a drain terminal and a gate terminal wherein the third mixer MOSFET receives an undivided and uncompensated phase locked loop oscillation signal and mixes the local oscillation frequency correction component in the current domain with the undivided and uncompensated phase locked loop oscillation signal received at the gate terminal of the third mixer MOSFET to create a compensated local oscillation at the drain terminal of the third mixer MOSFET; and

an output stage comprising an inductive coil coupled to the drain terminal of the third mixer MOSFET to convert the compensated local oscillation from the current domain to a voltage domain.

17 – 21 (Cancelled)